UNITED STATES PATENT APPLICATION

SOLDERING AN ELECTRONICS PACKAGE TO A MOTHERBOARD

INVENTOR

Daewoong Suh

Schwegman, Lundberg, Woessner & Kluth, P.A.
1600 TCF Tower
121 South Eighth Street
Minneapolis, MN 55402
ATTORNEY DOCKET SLWK 884.C25US1
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TECHNICAL FIELD

Some example embodiments of the present invention relate to connecting an electronic package to a motherboard, and more particularly, to soldering an electronic package to a motherboard.

BACKGROUND

The current paths in electronic assemblies that include processors are continually being required to handle ever-increasing amounts of current in order to power the processors. Processors typically require more power in order to operate at higher frequencies and to simultaneously perform numerous logic and memory operations. Each increase in processing speed and power generally carries a cost of increased heat generation within electronic assemblies that include processors. As processor power densities continue to increase, so too does the structural and thermal challenge of adhering electronic packages that include processors to a motherboard.

One example method of attaching an electronic package to a motherboard includes soldering the electronic package to the motherboard. One drawback with soldering the electronic package to the motherboard is that the various components contract at different rates during bonding due to differences in the coefficients of thermal expansion for the materials that form the electronic package, solder and motherboard. Since the electronic package, solder and motherboard contract at different rates, stress forms within the electronic package, solder and motherboard as the solder hardens to bond the electronic package to the motherboard.

Most conventional solders have re-flow temperatures around 183 °C and above. This relatively high re-flow temperature leads to significant temperature changes within the electronic package, solder and motherboard as the solder is re-flowed to connect an electronic package to a motherboard. The large temperature change generates significant expansion and contraction within the electronic

package, solder and motherboard as the solder is re-flowed and then cooled. The significant expansion and contraction causes stress within the components as the solder hardens. The stress within the components makes the electronic assemblies that include such components vulnerable to unwanted cracking.

One example relates to when a motherboard is mounted within a chassis that is shipped to an end user. The electronic package, solder and motherboard within such electronic assemblies are under stress such that they are particularly vulnerable to the shock and vibration forces generated during shipping.

In addition, the high re-flow temperature of some solders is simply not acceptable for many heat-sensitive devices (e.g., optoelectronic devices). Many electronic assemblies require a re-flow temperature that is less than 125 °C in order to connect an electronic package to a motherboard.

Devices that require a low re-flow temperatures leave only a small thermal window for assembly, as many devices operate at a working temperature around 80 °C. The small thermal window is problematic because there are a limited number of solders that have such a low melting temperature (T_m). In addition, many low T_m solders also include an undesirable toxic element (e.g., cadmium).

There are some conventional solders that have a T_m around 100 °C or less. Solders with such low T_m typically cannot be used in most electronic assemblies because their T_m is too close to, or below, the working temperature of many electronic assemblies.

One available alternative is to use adhesives to attach an electronic package to a motherboard. However, adhesives are limited in both thermal and electrical conductivity. Solder alloys are desirable because of their relatively high electrical and thermal conductivities.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a method that includes engaging a first contact on a motherboard with a second contact on an electronic package.

Figure 2 is a schematic section view of an electronic assembly before an electronic package is bonded to a motherboard.

Figure 3 is an enlarged schematic view illustrating an assembled portion of the electronic assembly shown in Figure 2.

Figure 4 is an enlarged schematic view similar to Figure 3 that illustrates another example embodiment of an assembled portion of the electronic assembly shown in Figure 2.

Figure 5 is a block diagram of an electronic system that incorporates the electronic assembly shown in Figure 2.

DETAILED DESCRIPTION

The following detailed description references the accompanying drawings. Like numerals describe substantially similar components throughout each of the drawings. Other embodiments may be used, and structural, logical, and electrical changes made. The integrated circuit described herein can be manufactured, used, or shipped in a number of positions and orientations.

Figure 1 illustrates one example embodiment of a method 10 that includes 15 engaging a first contact on a motherboard with a second contact on an electronic package. A portion of one of the first and second contacts is covered with an interlayer that has a lower melting temperature than both of the first and second contacts. The method further includes 20 bonding the first contact to the second contact by melting the interlayer to diffuse the interlayer into the first and second contacts. The bonded first and second contacts have a higher melting temperature than the interlayer before melting.

In some embodiments, 20 bonding the first contact to the second contact includes exposing the interlayer and the first and second contacts to an environment having a temperature greater than the melting temperature of the interlayer but below the melting temperature of the first and second contacts. As an example, the interlayer and the first and second contacts may be exposed to a temperature less than 125 °C. In addition, exposing the interlayer and the first and second contacts to

an environment may include maintaining the interlayer and the first and second contacts within the environment until (i) a portion of the interlayer diffuses into the first and second contacts; (ii) a majority of the interlayer diffuses into the first and second contacts; or (iii) the interlayer is substantially diffused into the first and second contacts.

Exposing the interlayer and the first and second contacts to an environment may also include exposing the interlayer and the first and second contacts to the environment for a period of time (e.g., minutes, hours or days). The interlayer and the first and second contacts may be exposed to the environment until the interlayer melts and then solidifies within the first and second contacts. It should be noted that the longer the interlayer and the first and second contacts are exposed to the environment, the more the interlayer may be diffused into the first and second contacts.

It should be noted that 20 bonding the first contact to the second contact by melting the interlayer to diffuse the interlayer into the first and second contacts may be done at a relatively low temperature depending on the type of interlayer. Bonding at a relatively low temperature reduces the stress in the bond between the electronic package and motherboard.

Once the interlayer is diffused into the first and second contacts, the re-flow temperature of the bonded first and second contacts is higher than the original melting temperature of the interlayer. The higher re-flow temperature allows an electronic assembly that includes an electronic package bonded to a motherboard to operate at higher temperatures.

The method 10 may further include 22 covering a portion of one of a first contact and a second contact with an interlayer (e.g., by electroplating, among other processes). It should be noted that 22 covering the portion of one of the first and second contacts with the interlayer may include (i) covering a portion of both of the first and second contacts with the interlayer; and/or (ii) covering all exposed portions of one of the first and second contacts with the interlayer.

Figure 2 illustrates an electronic assembly 50 that includes a motherboard 52 and an electronic package 54. The motherboard 52 includes a first contact 56 that is bonded to a second contact 58 on electronic package 54. Electronic assembly 50 further includes an interlayer 60 that is diffused within first contact 56 and second contact 58 when electronic package 54 is bonded to motherboard 52 (see Figures 3 and 4). The bonded first and second contacts 56, 58 have a higher melting temperature than the interlayer 60 before the interlayer 60 is diffused into the first and second contacts 56, 58.

In the example embodiment shown in Figure 2, first contact 56 is a pad and second contact 58 is a ball. It should be noted that first and second contacts 56, 58 may be any size, shape or geometry that permits the electronic package 54 to be bonded to motherboard 52.

In addition, first and second contacts 56, 58 may be made from the same material or different materials. Some example materials for first and second contacts 56, 58 include gold, silver, copper, tin and alloys comprised of any combination of tin, bismuth, lead and/or indium as long as the first and second contacts 56, 58 have a higher melting temperature than the interlayer 60. Some example materials for interlayer 60 include:

INTERLAYER (% BY WEIGHT)	(T_m) °C
52In-48Sn	118
66.3Bi-33.4In-0.3Zn	107.86
46Bi-34Sn-20Pb	96
52.2In-47.4Sn-0.4Zn	85.7
57Bi-26In-17Sn	79
66.3In-33.7Bi	72
66.9In-22.6Bi-0.5Zn	67.7
51In-32.5Bi-16.5Sn	60
49Bi-21In-18Pb-12Sn	58

Figure 3 shows that interlayer 60 is uniformly diffused within first and second contacts 56, 58. It should be noted that in other embodiments interlayer 60 may not be uniformly diffused into first and second contacts 56, 58. As an example, Figure 4 shows that interlayer 60 may be diffused within first and second contacts 56, 58 such that much of interlayer 60 is located near the area 63 where first contact 56 was mated with second contact 58. The degree of diffusion that interlayer 60 has within first and second contacts 56, 58 will depend on the temperature at which interlayer 60 is re-flowed, and the amount of time that interlayer 60 and first and second contacts 56, 58 are exposed to the re-flow temperature.

The types of materials that are selected for the interlayer 60 and the first and second contacts 56, 58 will depend on the application where the electronic assembly 50 is to be used. One important factor to consider when selecting materials is that there should be minimal formation of inter-metallic compounds between interlayer 60 and the first and second contacts 56, 58.

The melting temperature of the bonded first and second contacts 56, 58 is determined by (i) the types of materials that are used for interlayer 60 and first and second contacts 56, 58; and (ii) the degree of diffusion of interlayer 60 within first and second contacts 56, 58. In some embodiments, the bonded first and second contacts 56, 58 have a melting temperature greater than 150 degrees centigrade.

The size, type and alignment of electronic package 54 may vary depending on the design of electronic assembly 50. In addition, the components in electronic assembly 50 will be determined based on the space available and the application where electronic assembly 50 is to be used (among other factors).

As shown in Figure 2, electronic package 54 may include a die 61 that is mounted on a substrate 62. The die 61 and substrate 62 may be at least partially encapsulated by a protective material (not shown in Figures 2-4). Die 61 may be made of semiconducting material that has been separated from a wafer. Wafers may be made of semiconducting, non-semiconducting, or combinations of semiconducting and non-semiconducting materials.

It should be noted that die 61 may be a processor of any type. As used herein, processor means any type of circuit such as, but not limited to, a microprocessor, a microcontroller, a graphics processor or a digital signal processor. Die 61 may also be a custom circuit or an application-specific integrated circuit, such as a communications circuit for use in wireless devices such as cellular telephones, pagers, portable computers, two-way radios, and similar electronic systems.

FIG. 5 is a block diagram of an electronic system 70 incorporating at least one electronic assembly (e.g., electronic assembly 50 shown in Figure 2) described herein. Electronic system 70 may be a computer system that includes a system bus 72 which electrically couples the various components of electronic system 70 together. System bus 72 may be a single bus or any combination of busses.

Electronic assembly 50 is electrically coupled to system bus 72 and as discussed above may include any circuit, or combination of circuits. Electronic system 70 may also include an external memory 80 that in turn may include one or more memory elements suitable to a particular application. Some example memory elements include a main memory 82 in the form of random access memory (RAM), one or more hard drives 84, and/or one or more drives that handle removable media 86, such as diskettes, compact disks (CDs) and digital video disks (DVDs). The electronic system 70 may also include a display device 88, a speaker 89, and a controller 90, such as a keyboard, mouse, trackball, game controller, microphone, voice-recognition device, or any other device that inputs information into the electronic system 70.

In some embodiments, electronic system 70 further includes a voltage source 77 that is electrically coupled to electronic assembly 50. Voltage source 77 may be used to supply power to a die (e.g., a processor) that is within electronic assembly 50.

The methods and electronic assemblies described herein may be implemented in a number of different embodiments, including an electronic package, an electronic system, a computer system, and one or more methods of

fabricating an electronic assembly. The elements, materials, geometries, dimensions, and sequence of operations can all be varied to suit particular packaging requirements.

Figures 1-5 are merely representational and are not drawn to scale. Certain proportions thereof may be exaggerated while others may be minimized.

The method described above may provide a solution for bonding an electronic package to a motherboard. The method may reduce the stress within the bond that connects the electronic package and motherboard. The method may also allows an electronic assembly that includes the electronic package and motherboard to function at higher operating temperature than the temperature that is required to bond the electronic package to the motherboard. Many other embodiments will be apparent to those of skill in the art from the above description.